Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-14 (Cancelled).

15. (Previously Presented) An encryption circuit for simultaneously processing various encryption algorithms, the encryption circuit adapted to be coupled with a host computer system comprising:

an input/output module, including a microcontroller and memory, that handles data exchanges between the host computer system and the encryption circuit via a dedicated bus, the input/output module further including a flash memory and a static random access memory, the flash memory storing the code for a processor in the microcontroller, the processor copying contents of the flash memory into the static random access memory during startup,

an encryption module coupled with the input/output module, said encryption module controlling encryption and decryption operations, as well as storage of all sensitive information of the encryption circuit; and

isolation means between the input/output module and the encryption module, the isolation means makes the sensitive information stored in the encryption module inaccessible to the host computer system.

16. (Previously Presented) An encryption circuit according to claim 15, wherein the isolation means comprises a dual-port memory.

17. (Previously Presented) An encryption circuit according to claim 15, wherein the isolation means comprises a dual-port memory coupled between the input/output module and the encryption module, the dual-port memory is coupled to a first bus and simultaneously handles the exchange of data, commands and statuses between the input/output and encryption modules, and isolation between the input/output and encryption modules.

18. (Currently Amended) An encryption circuit ~~is~~ as set forth in claim 16, wherein the encryption module comprises:

a first encryption sub-module, dedicated to the processing of symmetric encryption algorithms, and being coupled with a first bus of the dual-port memory;

a second encryption sub-module, dedicated to the processing of asymmetric encryption algorithms and being coupled with the first bus of the dual-port memory and including a separate internal second bus isolated from the first bus of the dual-port memory; and

a CMOS memory, coupled with the dual-port memory via the first bus of the dual-port memory, containing the encryption keys.

19. (Cancelled).

20. (Previously Presented) An encryption circuit as set forth in claim 17, wherein the encryption module comprises:

a first encryption sub-module, dedicated to the processing of symmetric encryption algorithms, and being coupled with the first bus of the dual port memory;

a second encryption sub-module, dedicated to the processing of asymmetric encryption algorithms and being coupled with the first bus of the dual-port memory and including a separate internal second bus isolated from the first bus of the dual-port memory; and

a CMOS memory, coupled with the dual-port memory via the first bus of the dual-port memory, containing the encryption keys.

21. (Previously Presented) An encryption circuit according to claim 18, wherein the first encryption sub-module comprises an encryption component coupled with the dual-port memory via the first bus of the memory, comprising various encryption automata, respectively dedicated to the processing of symmetric encryption algorithms, and in that the second encryption sub-module comprises at least two encryption processors, respectively dedicated to the processing of asymmetric encryption algorithms, coupled with the encryption module via the internal second bus of the second sub-module and a bus isolator that isolates the second bus from the first bus of the dual-port memory.

22. (Previously Presented) An encryption circuit according to claim 21, wherein the encryption processors of the encryption module are of the CIP configuration.

23. (Previously Presented) An encryption circuit according to claim 21, wherein one of the two encryption processors is of the CIP type, and in that the other of the two encryption processors is of the ACE configuration.

24. (Previously Presented) An encryption circuit according to claim 21, wherein one of the two encryption processors is of the ACE configuration comprising a field programmable gate array (FPGA).

25. (Previously Presented) An encryption circuit according to claim 24, wherein the encryption component is of the SCE configuration.

26. (Previously Presented) An encryption circuit according to claim 25, wherein the encryption component comprises a field programmable array (FPGA).

27. (Previously Presented) An encryption circuit according to claim 26, wherein the second encryption sub-module comprises a flash memory PROM and an SRAM memory coupled with the second internal bus of the sub-module.

28. (Previously Presented) An encryption circuit according to claim 21, further comprising a CMOS memory containing security keys and security mechanisms that trigger a reset mechanism of the CMOS memory in case of an alarm.

29. (Previously Presented) An encryption circuit according to claim 15, wherein the microcontroller comprises:

an input/output processor and a PCI interface integrating DMA channels responsible for executing the data transfers between the host computer system and the circuit; and

the memory comprises the flash memory containing the code of the input/output processor and a PCI interface integrating DMA channels responsible for executing the data transfers between the host computer system and the circuit;

the flash memory containing the code of the input/output processor; and

the static random access memory that receives a copy of the contents of the flash memory upon startup of the input/output processor.

30. (Previously Presented) An encryption circuit according to claim 15, comprising a serial link connected to input basic keys through a secure path independent of the dedicated PCI bus, said link controlled by the encryption module.

31. (Previously Presented) An encryption circuit according to claim 30, wherein the serial link (SL) allows downloading of proprietary algorithms into the first encryption sub-module.

32. (Original) An encryption circuit as set forth in claim 15, further including a card supporting the circuit.

33. (Original) An encryption circuit as set forth in claim 18, further including a card supporting the circuit.

34. (Original) An encryption circuit as set forth in claim 21, further including a card supporting the circuit.